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# Claims

[c1] 1. A flash memory cell, comprising:

a substrate;

a stack gate structure formed on said substrate, said stack gate structure including a select gate dielectric layer, a select gate, and a gate cap layer, said select gate dielectric layer being formed between said substrate and said select gate, said gate cap layer being formed on said select gate;

a spacer formed along a sidewall of said select gate;

a control gate formed on one side of said stack gate structure and connected to said stack gate structure;

a floating gate formed between said control gate and said substrate and including a recess;

an inter-gate dielectric layer formed between said control gate and said floating gate;

a tunneling dielectric layer formed between said floating gate and said substrate; and

a drain region and a source region formed in said substrate, wherein said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively.

[c2] 2. The flash memory cell of claim 1, wherein a top surface of said floating gate layer is positioned between a top surface of said spacer and a top surface of said cap layer.

[c3] 3. The flash memory cell of claim 1, wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide.

[c4] 4. A flash memory cell array, comprising:
a substrate;
a plurality of flash memory cell structures formed on said substrate, wherein each of said flash memory cell structures including
a stack gate structure formed on said substrate and including a select gate dielectric layer, a select gate, and a gate cap layer, wherein said select gate dielectric layer is formed between said substrate and said select gate, and said gate cap layer is formed on said select gate;
a spacer formed along a sidewall of said select gate;
a control gate formed on the one side of said stack gate structure and connected to said stack gate structure;
a floating gate formed between said control gate and said substrate;
an inter-gate dielectric layer formed between said control gate and said floating gate, wherein said control gate and said floating gate constitute a stack structure;

a tunneling dielectric layer formed between said floating gate and said substrate; and

a drain region and a source region formed in said substrate, said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively;

wherein said stack gate structure juxtaposes alternatively with said stack structure in said flash memory cell structures.

[c5] 5. The flash memory cell array of claim 4, wherein a top surface of said floating gate layer is positioned between a top surface of said spacer and a top surface of said gate cap layer.

[c6] 6. The flash memory cell array of claim 4, wherein said floating gate includes a recess, and said recess is substantially filled with said control gate.

[c7] 7. The flash memory cell array of claim 4, wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide.

[c8] 8. A method for fabricating a flash memory cell array, comprising:

providing a substrate having a device insulating structure;

forming a plurality of stack gate structures on said substrate, and said stack gate structure including a select gate dielectric layer, a select gate, and a gate cap layer, wherein said select gate dielectric layer being formed between said substrate and said select gate, said gate cap layer being formed on said select gate;

forming a tunneling dielectric layer on said substrate;

forming a spacer along a sidewall of said select gate;

forming a floating gate between each of said stack gate structures, wherein said floating gate includes a recess and connected to said stack gate structure, and an upper sidewall of the floating gate is defined as between a top surface of said gate cap layer and a top surface of said select gate;

forming an inter-gate dielectric layer on said floating gate;

forming a control gate to fill at least one gap between each of said stack gate structures;

removing a portion of said stack gate structures excluding a predetermined area of said flash memory cell array; and

forming a drain region and a source region in said substrate, said drain region and said source region being on the one side and the other side out of said control gates and said stack gate structures respectively.

[c9] 9. The method for fabricating a flash memory cell array of claim 8, wherein the step of forming said floating gate further comprises:
forming a first conducting layer on said substrate;
forming a material layer on said first conducting layer, and said material layer filling at least one gap between each of said stack gate structures;
removing a portion of said material layer until a top surface of said material layer is between a top surface of said cap layer and a top surface of said select gate;
removing a first portion of said first conducting layer by using said material layer as a mask;
removing the material layer; and
removing a second portion of said first conducting layer on said device insulating structure to form said floating gate.

[c10] 10. The method for fabricating a flash memory cell array of claim 9, wherein said material layer includes a photoresist layer.

[c11] 11. The method for fabricating a flash memory cell array of claim 9, wherein said material layer includes an anti-reflecting coating layer.

[c12] 12. The method for fabricating a flash memory cell array of claim 9, wherein said material layer step is formed by

performing a spin coating process.

[c13] 13. The method for fabricating a flash memory cell array of claim 9, wherein the portion of said material layer is removed by performing an etching back process.

[c14] 14.The method for fabricating a flash memory cell array of claim 8, wherein the step of forming said control gate comprises:
forming a second conducting layer on said substrate; and
removing a portion of said second conducting layer, until a top surface of said gate cap layer is exposed, to form said control gate.

[c15] 15. The method for fabricating a flash memory cell array of claim 14, wherein the portion of said second conducting layer is removed by performing an etching back process or a chemical mechanical polishing process.

[c16] 16. A method for fabricating a flash memory cell array, comprising:
providing a substrate having a device insulating structure;
forming a plurality of stack gate structures on said substrate, and each of said stack gate structure including a select gate dielectric layer, a select gate, and a gate cap

layer, wherein said select gate dielectric layer is formed between said substrate and said select gate, said gate cap layer is formed on said select gate;

forming a tunneling dielectric layer on said substrate;

forming a spacer along a sidewall of said select gate;

forming a floating gate between each of said stack gate structures;

forming an inter-gate dielectric layer on said floating gate;

forming a control gate in at least one gap between each of said stack gate structures;

removing a portion of said stack gate structures excluding a predetermined area of said flash memory cell array; and

forming a drain region and a source region in said substrate, said drain region and said source region being on the one side and the other side of said control gates and said stack gate structures respectively.

[c17] 17. The method for fabricating a flash memory cell array of claim 16, wherein the step of forming said floating gate comprises:

forming a first conducting layer on said substrate;

removing a first portion of said first conducting layer until a top surface of said first conducting layer is between a top surface of said gate cap layer and a top sur-

face of said select gate; and
removing a second portion of said first conducting layer on said device insulating structure to form said floating gate.

[c18] 18. The method for fabricating a flash memory cell array of claim 16, wherein the step of removing the portion of said conducting layer comprises performing an etching back process.

[c19] 19. The method for fabricating a flash memory cell array of claim 16, wherein the step of forming said control gate comprises:
forming a second conducting layer on said substrate; and
removing a portion of said second conducting layer, until a top surface of said cap layer is exposed, to form said control gate.

[c20] 20. The method for fabricating a flash memory cell array of claim 19, wherein the step of removing the portion of said second conducting layer comprises performing an etching back process or a chemical mechanical polishing process.

[c21] 21. A method of operating a flash memory cell array, said flash memory cell array comprising a serial connec-

tion of a plurality of flash memory cells, a drain region and a source region in a substrate and positioned on the one side and the other side out of said control gates and said stack gate structures respectively, each of said flash memory cell including a stack gate structure having a select gate, a control gate positioned and connected on the one side of said stack gate structure, a floating gate positioned between said control gate and said substrate, wherein said stack gate structure of said plurality of flash memory cell structures juxtaposing alternatively with a stack structure having said control gate and said floating gate, said method comprising:

before programming said flash memory cell array, applying a first voltage, a second voltage, and a third voltage to said source region, said select gates, and said control gates respectively and applying substantially 0 voltage to said drain region and said substrate, in order to turn on the channels of said flash memory cells;

during programming said flash memory cell array, applying said first voltage, a fourth voltage, said second voltage, a fifth voltage, said third voltage, and substantially 0 voltage to said source region, said select gates of selected said flash memory cells, said select gates of non-selected said flash memory cells, said control gates of said selected flash memory cells, said control gates of said non-selected flash memory cells, and said substrate

respectively, to cause source-side injection in order to inject electrons into said selected flash memory cells to program said selected flash memory cells;

during reading said flash memory cell array, applying substantially 0 voltage, a sixth voltage, a seventh voltage, and a eighth voltage to said source region, said select gates, said control gates, said drain region respectively; and

during erasing said flash memory cell array, applying substantially 0 voltage to said source region and said select gates and said control gates, and applying a ninth voltage to said substrate, to cause Fowler-Nordhem tunneling in order to push electrons from said floating gates into said substrate to erase said flash memory cell array.

[c22] 22. The method of operating a flash memory cell array of claim 21, wherein said first voltage is substantially equal to 4.5 V.

[c23] 23. The method of operating a flash memory cell array of claim 21, wherein said second voltage is substantially equal to 7 V.

[c24] 24. The method of operating a flash memory cell array of claim 21, wherein said third voltage is substantially equal to 11 V.

[c25] 25. The method of operating a flash memory cell array of claim 21, wherein said fourth voltage is substantially equal to 1.5 V.

[c26] 26. The method of operating a flash memory cell array of claim 21, wherein said fifth voltage is substantially equal to 9 V.

[c27] 27. The method of operating a flash memory cell array of claim 21, wherein said sixth voltage is substantially equal to 4.5 V.

[c28] 28. The method of operating a flash memory cell array of claim 21, wherein said seventh voltage is substantially equal to 1.5 V.

[c29] 29. The method of operating a flash memory cell array of claim 21, wherein said eighth voltage is substantially equal to 1.5 V.

[c30] 30. The method of operating a flash memory cell array of claim 21, wherein said ninth voltage is substantially equal to 11 V.